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"Functioning of electronic devices with dimensions on the nanometer scale"

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Abstract

For more than a decade intense research on semiconductor nanowires has been ongoing, due to the potential that these structures offer for coming generations of electronic, optoelectronic and biosensor applications. However, if large-scale production of nanowire-based devices is to be realized better control and understanding of the nanowire growth process needs to be achieved. Today particle-assisted growth is the most widely used method for production of epitaxial semiconductor nanowires. Nanoparticles of various different materials have been used to seed the growth of nanowires, but gold particles are by far the most common choice since gold is superior to other materials in most cases of nanowire growth. Although several nanowire growth models discuss the role of the seed particle, no clear understanding of why gold is such a suitable seed particle material exists. Furthermore, several different generation and deposition methods have been used to produce gold seed particles, but the effect of gold particle manufacturing method on nanowire growth is yet unclear.

Introduction:

Rational design and synthesis of nanoscale materials is critical to work directed toward understanding fundamental properties, creating nanostructured materials, and

developing nanotechnologies. In this regard, we have developed a general approach to controlled synthesis of a broad range of semiconductor NWs via a metal cluster-catalyzed vapor–liquid–solid (VLS) growth mechanism. Here, the catalyst is envisioned as a nanocluster or nanodroplet that defines the diameter of the NWs and serves as the site that directs preferentially the addition of reactant to the end of a growing NW much like a living polymerization catalyst directs the addition of monomers to a growing polymer chain (Fig. 1). Within this framework, a broad range of semiconductor NWs, typically with diameters on the order of 10 nm, and lengths extending up to tens of micrometers can be rationally and predictably synthesized in single crystal form with all key parameters, including chemical composition, diameter, and length, and physical properties controlled.

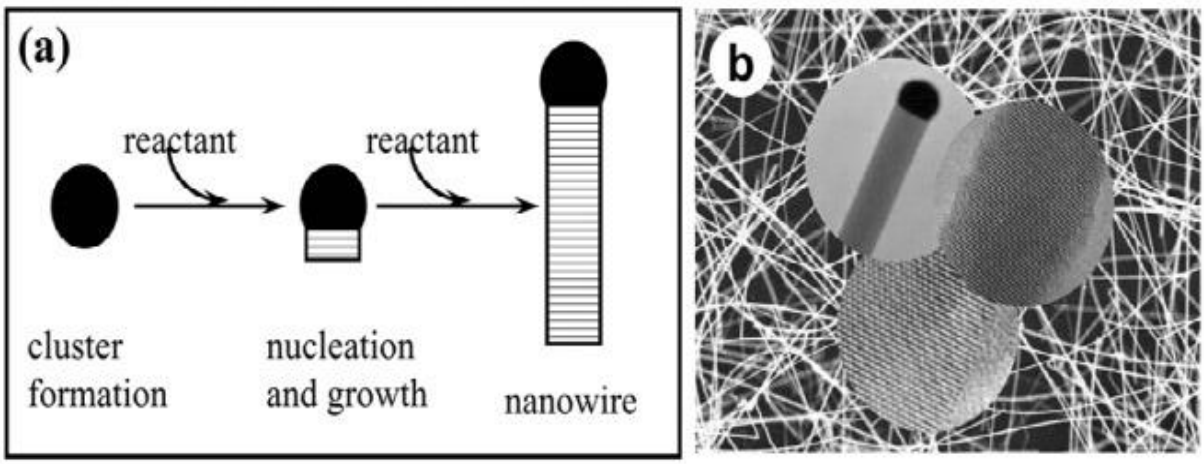

Fig.1: NW building blocks.

The second approach, denominated “top-down”, downscales the structuring of surfaces into the nanoscale by using currently available methods, usually highend lithography processes applied in the semiconductor industry. Although the “bottom-up” approach is quite interesting since it leads to completely new structures, it lacks of a real spatial control of the patterning process and requires additional characterization methods.

The most versatile “top-down” approach to get access to the nanoscale is the lithography of surfaces by scanning probe microscopy (SPM), which relies on the modification of chemical, electrical or mechanical properties of a surface by using a proximal probe. SPM based lithography achieves a high fabrication control over both direction and position. Additionally,

SPM offers the possibility of in situ ultra-high resolution characterization of the fabrication process and resulting surface structure. The success of SPM also relies on the fact that its application for imaging is not only restricted to topography measurement, but also offers a plethora of possibilities to characterize different surface properties, including the local acquisition of spectroscopy data reaching the single-molecular level.

2. Related work

Direct assembly of highly integrated functional electronic circuits based on NWs requires (1) the development of new device concepts with scalable device configuration and (2) high yield assembly of these devices with controllable functional properties. The crossed NW matrix represents an ideal configuration since the critical device dimension is usually defined by the cross-point and can be readily scaled down to nanometer level, and crossed NW configuration itself is naturally a scalable architecture and thus enables the possibility of massive system integration. Moreover, the crossed NW matrix is a versatile structure and can be configured into a variety of critical device elements, such as diodes and transistors. For example, a p-n diode can be obtained by simply crossing a p- and n-type NW as demonstrated in the cases of p-Si/n-Si, p-InP/n-InP, p-InP/n-CdS and p-Si/n-GaN materials. Electrical measurements of such crossed junctions show clear current rectification across the junction and linear current behavior in individual NWs, demonstrating the formation of p-n diode at the crossing point. To gauge the reproducibility of these assembled NW p-n diodes, we have studied a large number of p-n junctions assembled from p-Si NWs and n-GaN NWs. I-V measurements made on over 100 crossed p-Si/n-GaN NW devices show that over 95 % of the junctions exhibit current rectification with turn-on voltages of around 1.0 V. Reproducible assembly of crossed NW structures with predictable electrical properties contrasts sharply with results from NT-based device, and readily enabled us also to explore the assembly and properties of integrated p-n diode arrays. Significantly, electrical transport measurements made on a typical 4 by 1 crossed p-Si/n-GaN junction array show that the four nanoscale cross-points form independently addressable p-n diodes with clear current rectification and similar turn-on voltages.

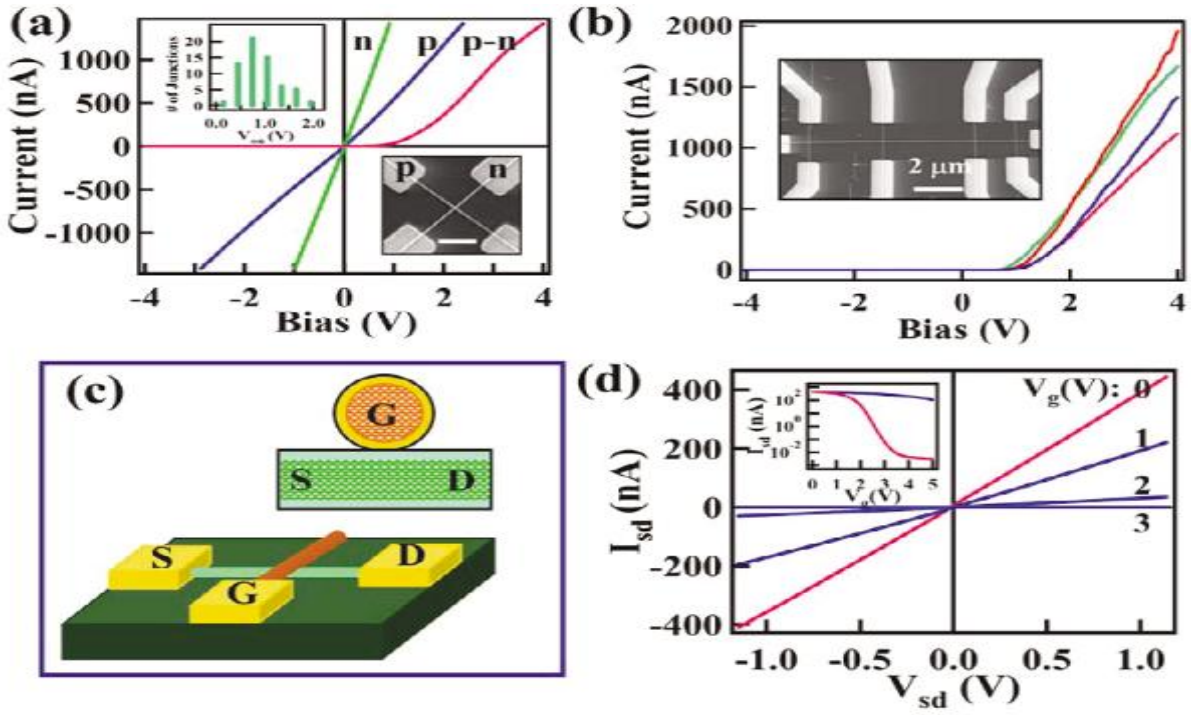

Fig. 2 Crossed nanowire devices.

The single system configuration, in which the antiresonant frequencies are affected by the tip-sample interaction, corresponds to a distributed force input and cantilever slope output. Additionally, this system configuration is non-minimum in phase, which implies a limitation of the bandwith of a hypothetical model based controller. Using the infinite product expansion of the transfer functions we have obtained an analytical expression of all system poles and zeros, which allows for the study of system stability, range of non-minimum phase behavior, and step

response. In particular, the study of the step response of the system has a direct application to the study of AFM force spectroscopy. The shift of resonant and antiresonant frequencies with varying contact stiffness is of critical importance for dynamical methods of AFM based mechanical nanolithography since it influences the magnitude of the applied load, and therefore, the indentation depth as demonstrated in acoustical force nanolithography.

2.1 Nanoscale logic gates and computational circuits

High-yield assembly of crossed NW p-n diodes and cNW-FETs from p-Si and n-GaN materials enables more complex functional electronic circuits, such as logic gates to be produced. Logic gates are critical blocks of hardware in current computing systems that

produce a logic-1 and logic-0 output when the input logic requirements are satisfied. Diodes and transistors represent two basic device elements in logic gates. Transistors are more typically used in current computing systems because they can exhibit voltage gain. Diodes do not usually exhibit voltage gain, although they may also be desirable in some cases, for example, the circuit architecture and constraints on the assembly of nanoelectronics might be simplified using diodes since they are two-terminal devices, in contrast to three terminal transistors. In addition, by combining the diodes and transistors in logic circuits, it is possible to achieve high voltage gain, while simultaneously maintaining a simplified device architecture.

To demonstrate the flexibility of these NW device elements, we have investigated both diode- and FET-based logic. For example, a two-input logic OR gate was realized using a 2(p) by 1(n) crossed NW p-n diode array. When either of the input to the p-NW is high, a high output is obtained at the n-NW as the p-n diode is forward biased; a low output is only achieved when both inputs are low; and thus realizing the same function as a conventional logic “OR” gate. A logic AND gate was also assembled from two p-n diodes and one cNW-FET and a logic NOR gate with gain over 5 was assembled from three cNW-FETs in series . Importantly, logic OR, AND, and NOR gates form a complete set of logic elements and enable the organization of virtually any logic circuits. For example, NW logic gates have been interconnected to form an XOR gate and a logic half adder, which was used to carry out digital computations in a way similar to conventional electronics.

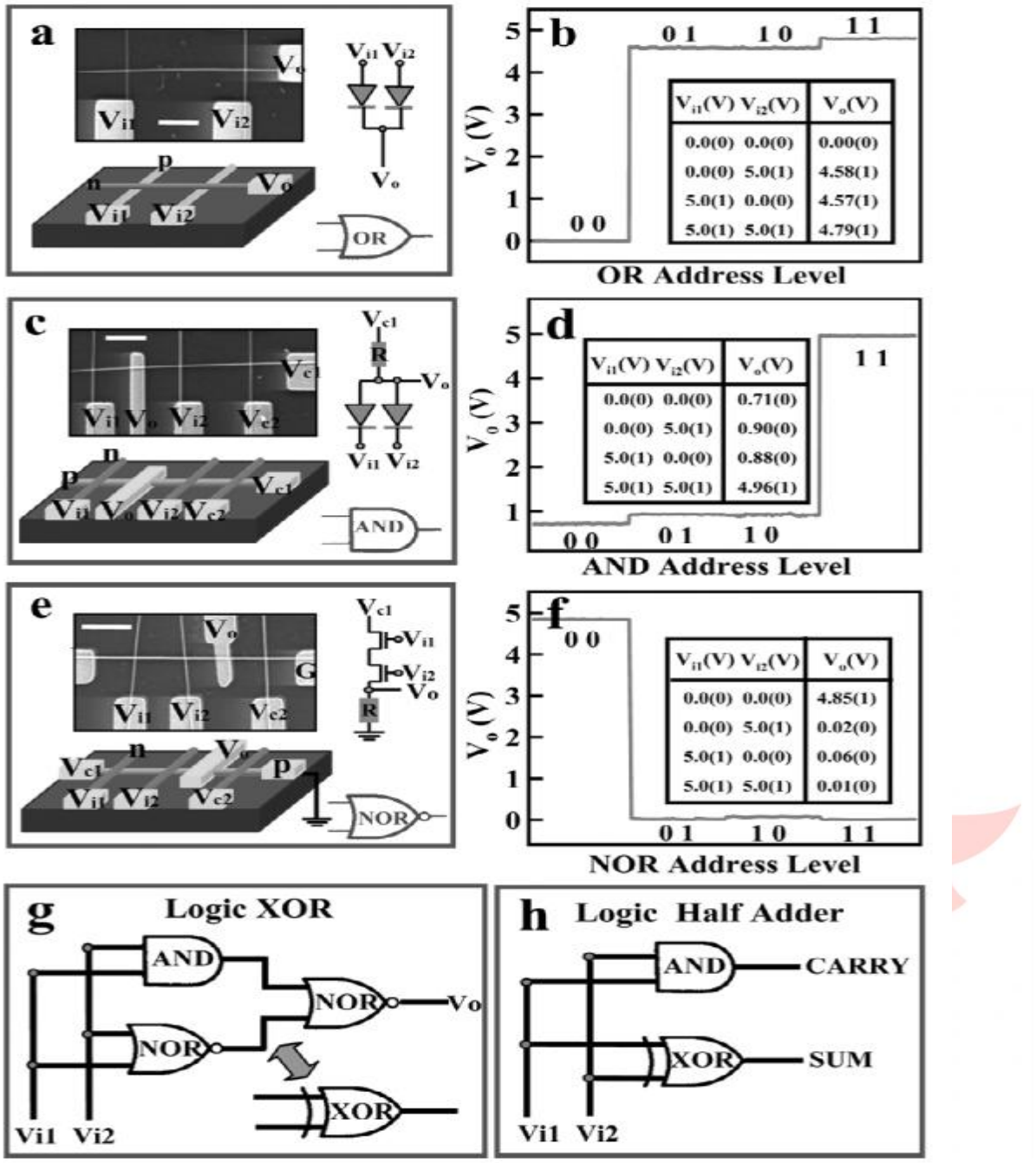

Fig 3: Nanoscale logic gates.

3. Objectives

The main objective of this study is to describe the development of an alternative device structure having minimal device area, and discusses the electrical properties of devices fabricated with this structure. The study also describes the opportunities for new memory technologies are explored, and some emerging organic memory technologies are reviewed. The requirements for the integration of organic memory devices into high-speed and high-density circuits are considered.

4. Hypotheses

The increasing demand for electronic memory, driven by sales of personal computers and mobile electronic devices, provides a significant incentive for the continued development of high-performance memory. Although some data-storage technologies, such as digital video disks (DVDs), offer almost limitless, inexpensive data storage, their ability to alter data after it is stored is limited. For most applications, memory in which the stored data can be readily altered (programmed) is desirable. Currently, the programmable-memory market is dominated by four technologies. The first technology is the hard disk drive, which stores data in the local polarization of a paramagnetic disk. This data is accessed and programmed by a miniature antenna (or head) as the disk is rotated. Hard disks are nonvolatile, meaning that a stored state is retained without applied power. Although very inexpensive, the mechanical rotation limits the hard disk's operating speed and ability to withstand physical vibrations and shocks.

5. Conclusion

The disparity of performance and cost characteristics between the memory technologies allows each to fill an application niche (or niches) without significant competition from the other technologies. For example, SRAM is used in applications that require extremely high data turnover and therefore short access/program times (such as the in cache memory of a computer processor), while a computer hard disk is used as a large, long-term repository for files that are used infrequently. In mobile electronic devices, which represent a fast-growing segment of the memory market, nonvolatile memory is especially appealing because it allows long-term data storage without drawing battery power. Other advantages include the ability to withstand unexpected power outages without data loss, and the potential to bypass the lengthy boot sequences upon startup that are required by volatile memories. Eliminating lengthy boot sequences enables further decreases in power usage by making frequent

transitions to and from power-saving standby modes possible without disrupting the user. A technology with these attributes could potentially be used for any memory application, replacing all other technologies and acting as a "universal" memory [9]. In region II, the hypothetical memory could compete with DRAM, SRAM, and flash memory, potentially replacing these technologies.

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